ABSTRACT OF THE DISCLOSURE

A data processing apparatus includes address generation circuit, an address translation circuit, a selection circuit, a memory, a shifter, an ALU and a mixing circuit. The address generation circuit generates a logical address for data including 10 bit imaginary part, 10 bit real part and 12 bit reserved part. The address translation circuit translates the logical address into a physical address for data including 16 successive bits of the imaginary part and the real part. The selection circuit generates a selection signal in response to the logical address. The memory for storing 16 bits of data in accordance with the physical address. The shifter shifts the received data from the memory in response to the selection signal. The ALU processes an arithmetic operation in response to the shifter output. The mixing circuit mixes the data received from the memory and the ALU and outputs the mixed data to the memory.